5V Input 3A(4A Peak) 1.25MHz Synchronous Step-Down DC/DC Converter

DESCRIPTION

The MT8103 is a 1.25MHz, 3A continued (4A Peak) constant on-time (COT) controlled synchronous step-down converter. It can operate with input voltage from 2.5V to 5.5V and provide output range from 0.6V to input level. The constant on-time control scheme simplifies loop compensation and offers excellent load transient response. The high gain error amplifier in the control loop provides excellent load and line regulation. Proprietary adaptive on-time helps MT8103 to achieve nearly constant switching frequency across load range. MT8103 has cycle-by-cycle current limit and hiccup mode to protect over-load or short circuit fault conditions.

MT8103 is available in low profile 6 leads SOT563.

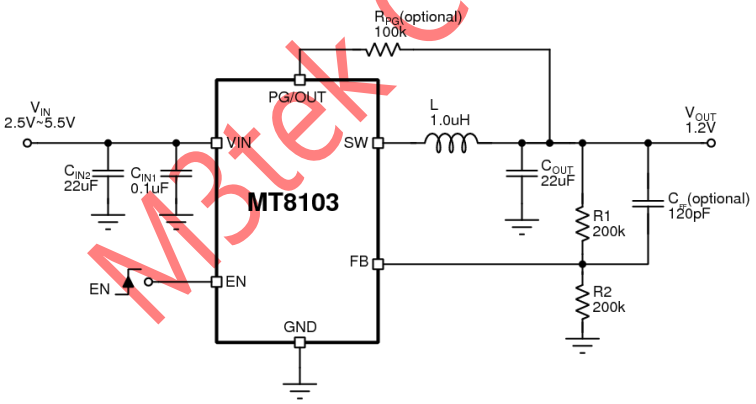
FEATURES

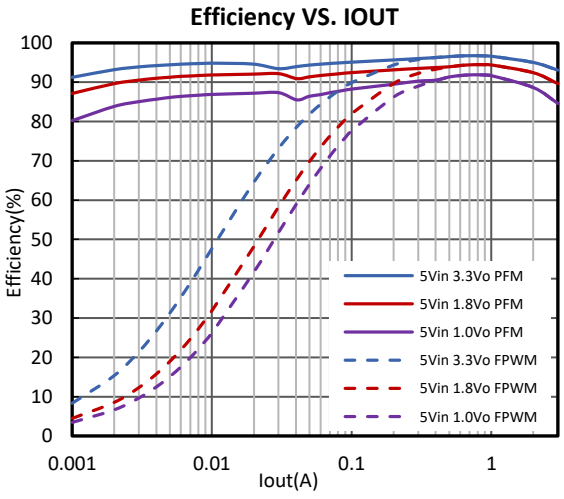
- Wide Input Range from 2.5V to 5.5V
- 3A Continuous Output Current (4A Peak)
- Proprietary Fast Transient Constant On Time Architecture Stable with low ESR Ceramic Output Capacitors
- +/- 1% 0.6V Feedback Voltage
- 1.25MHz Switching Frequency
- Up to 95% Efficiency
- 18μA Quiescent Current (MT8103N) PFM mode
- 100% Duty Cycle Operation
- Built-in Power Switches
  HS/LS MOS:55mΩ/25mΩ @5V VIN
- Internal 1msec Soft-Start
- Cycle-by-cycle Current Limit Protection
- Over-Load and Short Circuit Hiccup Mode
- Open Drain Power Good Indication
- Output Discharge
- Thermal Shutdown Protection
- Available in Small SOT563
- Pb-Free RoHS Compliant

APPLICATIONS

- Solid-State and Hard Disk Drives
- Smart Phone and Tablets
- Wi-Fi RF Modules
- IoT peripherals device

TYPICAL APPLICATION





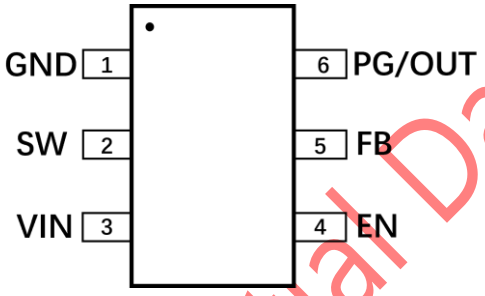
5V Input 3A(4A Peak) 1.25MHz Synchronous Step-Down DC/DC Converter

ORDERING INFORMATION

Part No.	Marking	Temp. Range	Remark	Package	MOQ
MT8103NSLR	8103 YWX	-40°C ~+85°C	PFM Mode	SOT563	5000/Tape & Reel
MT8103ASLR	103A YWX	-40°C ~+85°C	FPWM Mode	SOT563	5000/Tape & Reel

Note: Y: Year, W: Week, X Control Code

PIN CONFIGURATION

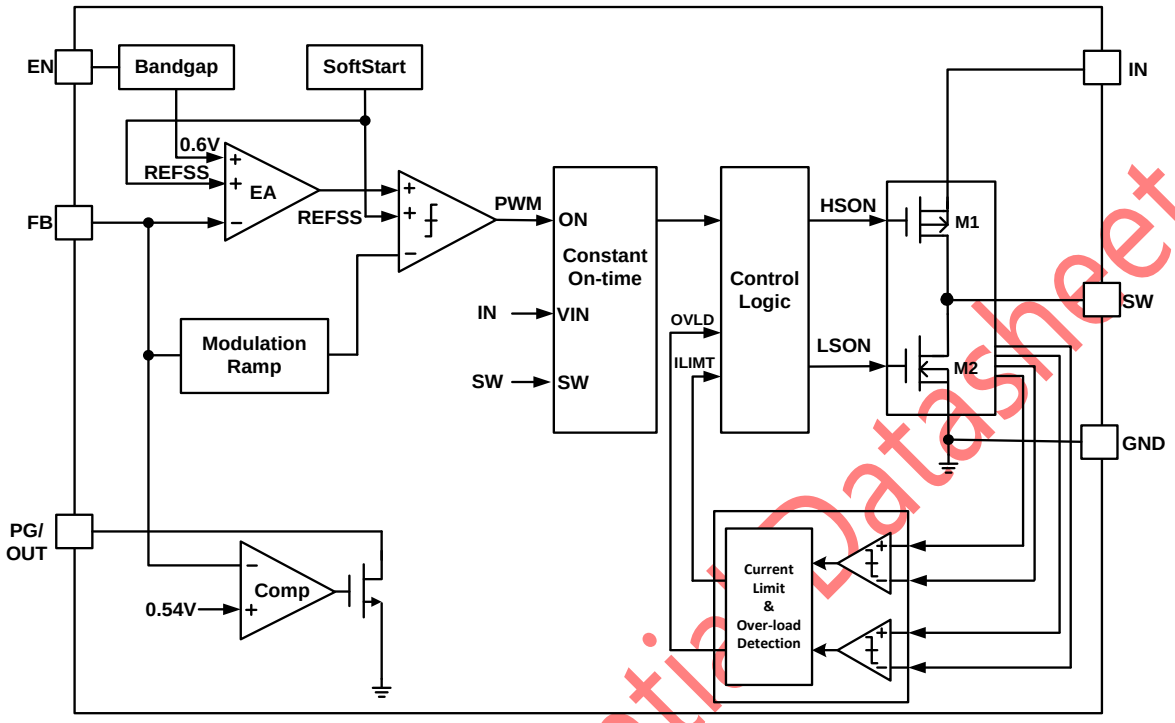


Top View SOT563

PIN DESCRIPTION

SOT563 Pin No.	Symbol	Description
1	GND	Power ground.
2	SW	Switching pin, connect to external inductor.
3	VIN	Input Supply Voltage.
4	EN	Don't float this pin. This pin has a pull-down resistor of typically 1MΩ to GND. • Drive EN above 1.5V to turn on the converter. • Drive EN below 0.4V to turn off the converter and discharge output.
5	FB	Feedback voltage input, connect to external feedback resistors
6	PG/OUT	Power Good Open-drain Output. Connect a 100kΩ pull-up resistor to VIN or VOUT. If no need PG function, leave the pin floating or connect to Output directly.

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Rating(Reference to GND) (Note1)

V_{IN} ..... -0.3V to +6.5V
V_{SW} ..... -0.3V to V_{IN} +0.3V
Dynamic V_{SW} in 10ns Duration ..... -2V to V_{IN} +2V
The other Pins..... -0.3V to +6.5V

Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... 260°C
ESD ..... Class 2

Recommend Operating Conditions (Note2)

Input Voltage (V_{IN}) .....+2.5V to +5.5V
Output Voltage (V_{OUT}) .....+0.6V to V_{IN}

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Range(Tj) ... -40°C to +125°C

Thermal information(Note3, 4)

Maximum Power Dissipation(T_A=25°C)
SOT563_6L.....1.6W

Thermal Resistance(θ_{JA}) .....78°C/W
Thermal Resistance(θ_{JC}) .....43°C/W

Note (1): Stress exceeding those listed “Absolute Maximum Ratings” may damage the device.
Note (2): The device is not guaranteed to function outside of the recommended operating conditions.
Note (3): Measured on JESD51-7, 4-Layer PCB.
Note (4): The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\_MAX}= (T_{J\_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN}=5V, unless otherwise noted. Typical values are at V_{IN} = V_{EN} = 5V.

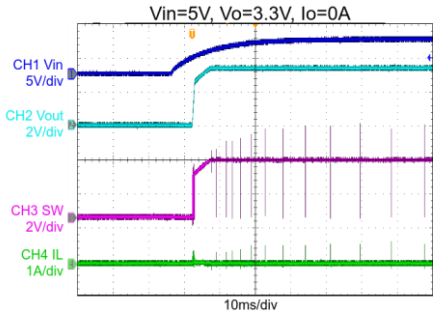
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		2.5		5.5	V
Shutdown Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = 5.5V		0.1	1	μA
Input Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Increasing	2.2	2.35	2.5	V
Input Under Voltage Lockout Hysteresis	V_{UVHYS}			300		mV
Input Over Voltage Lockout Threshold	V_{INOV}			6.35		V
Input Over Voltage Lockout Hysteresis	V_{INOVHY}			600		mV
Quiescent Current	I_Q	V_{FB} = 0.63V (PFM_MT8103N)		18	24	μA
		V_{FB} = 0.63V (PWM_MT8103A)		600		μA
Feedback Voltage	V_{FB}		594	600	606	mV
Feedback Current	I_{FB}		-50	1	+50	nA
HS Switch Peak Current Limit	I_{LIM}			6.4		A
HS Switch On Resistance	R_{ONHS}	V_{IN}=5V		55		mΩ
LS Switch On Resistance	R_{ONLS}	V_{IN}=5V		25		mΩ
LS Switch Negative Current Limit	I_{NEG}	PWM MT8103A		-1.8		A
LS Switch Zero-Current Detection	I_{ZRO}	PFM MT8103N		50		mA
HS Leakage Current	I_{LKHS}	V_{IN} = 5.5V, V_{EN} = V_{SW} = 0V		0.1	2	μA
LS Leakage Current	I_{LKLS}	V_{IN} = V_{SW} = 5.5V, V_{EN} = 0V		0.1	2	μA
PWM Switching Frequency Note5		I_{IOUT} = 1A		1.25		MHz
PGOOD Output Low Voltage	V_{PGLO}	V_{FB} =0.5V, sink 1mA		0.2	0.3	V
PGOOD Output Leakage Current	I_{LKPG}	V_{FB} = 0.63V , VPGOOD = V_{IN} = 5.5V		0.01	0.2	μA
PGOOD Under Voltage Rise Threshold	P_{CTPGR}	V_{FB} with ramp up from under voltage		-10		%
PGOOD Under Voltage Fall Threshold	P_{CTPGF}	V_{FB} ramp down from regulation		-15		%
PGOOD Delay	T_{DPGD}	PGOOD going High to Low		45		μs
EN On Threshold	V_{ENON}	V_{EN} ramp up	1.5			V
EN Off Threshold	V_{ENOFF}	V_{EN} ramp down			0.4	V
EN Internal Pull Down Resistor	R_{EN}			1		MΩ
Output Discharging Resistance		V_{EN} = 0V, V_{OUT} = 1V		20		Ω
Soft Start Time	T_{SS}			1		ms
Thermal Shutdown				160		℃
Thermal Shutdown Hysteresis				30		℃

Note5: Switch Frequency (steady state) is Guaranteed by the formula F_{SW}=VOUT/(VIN*TON)

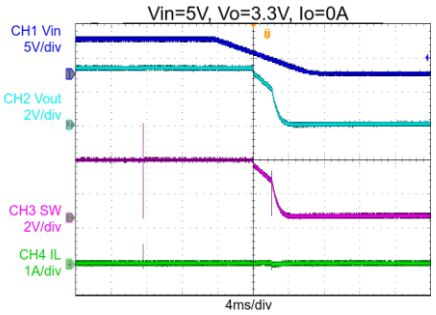
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN}=22uF+0.1uF, C_{OUT}=22uF, C_{FF}=120pF, L=1.0uH, TA =25°C.

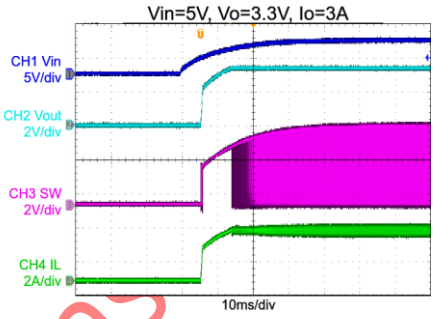
Vin Power On



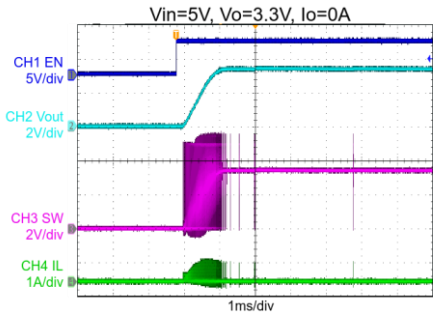
Vin Power Off



Vin Power On



EN On



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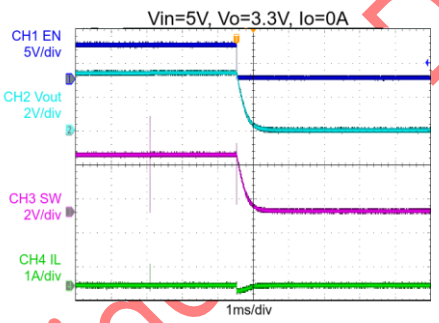
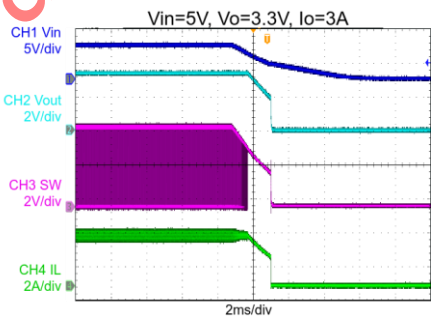
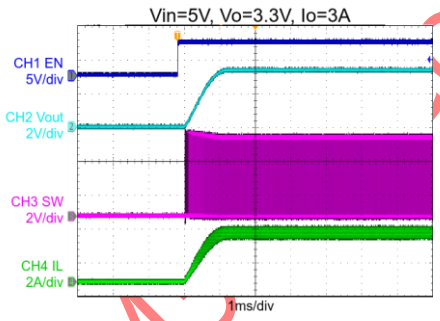


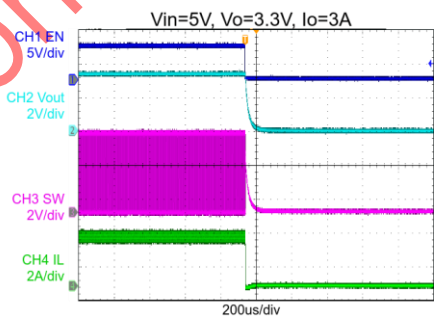
Vin Power Off



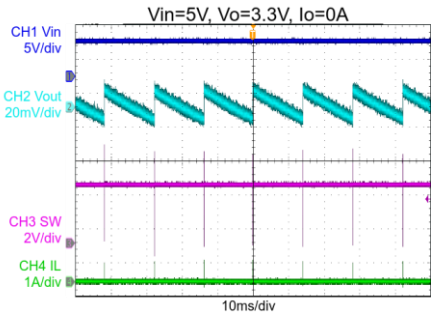
EN On



EN Off



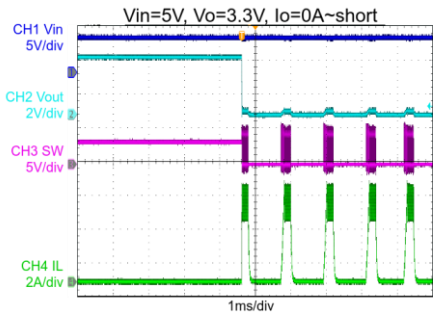
Steady State Test



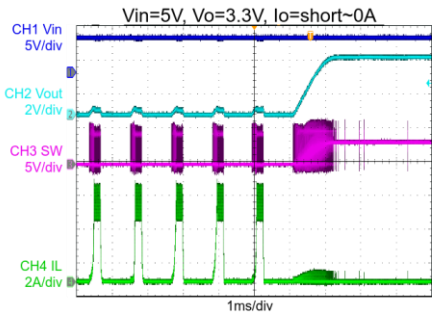
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN}=22uF+0.1uF, C_{OUT}=22uF, C_{FF}=120pF, L=1.0uH, TA =25°C.

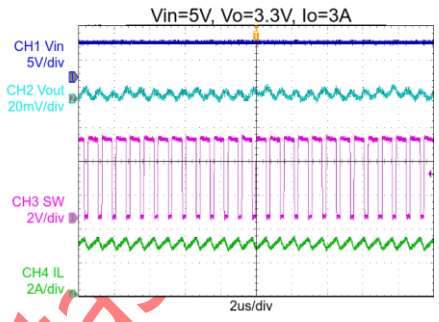
Short Protection



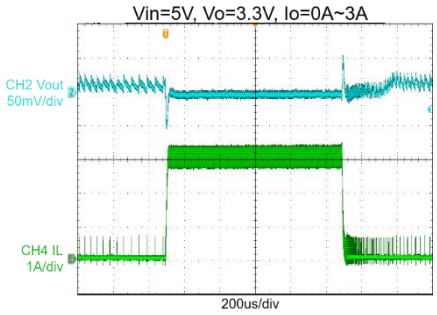
Short Circuit Recovery



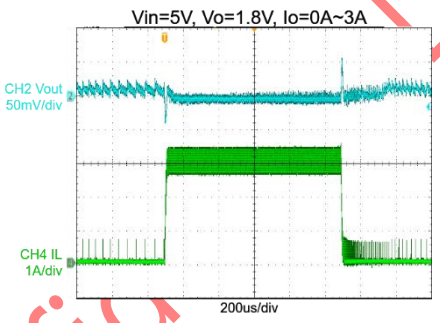
Steady State Test



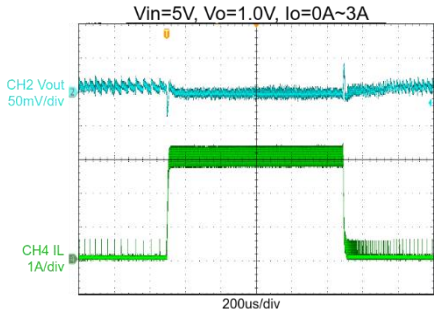
Load Transient Response



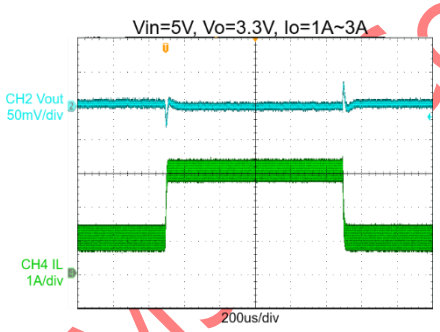
Load Transient Response



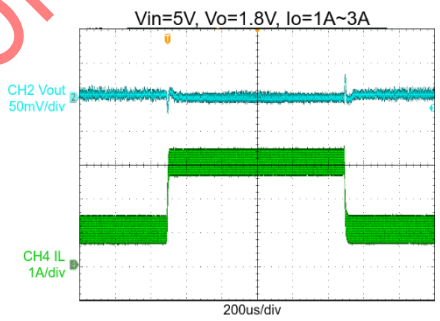
Load Transient Response



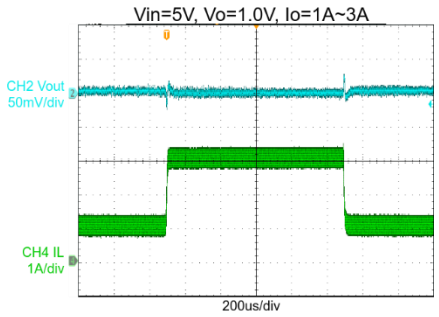
Load Transient Response



Load Transient Response



Load Transient Response



OPERATION

MT8103 is a constant on-time control synchronous step-down converter that offers excellent transient response over a wide range of input voltage. It achieves superior light-load efficiency with extremely low quiescent current.

Constant On-time Control

Constant on-time control step-down converters turn on HS immediately when FB droops below reference. The HS is turned on for a pre-determined period (on-time) of time to ramp up the inductor current, and then the LS will be turned on to ramp down the inductor current. The cycle repeats itself if FB droops below reference again. MT8103 uses proprietary technique to take into account the load current impact and adjusts the on-time accordingly to achieve a constant switching frequency over entire load current range.

For MT8103, the on-time is approximately:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{FSW}$$

Due to its immediate response on FB voltage droop and simplified loop compensation, constant on-time offers a superior transient response compare to traditional fixed frequency PWM control step-down converters.

Light Load Operation (MT8103N only)

In light load condition where the converter operates in discontinuous mode, MT8103N cuts down its quiescent current to as low as 18uA and achieves excellent light load efficiency.

Enable

When input voltage is above the Under-Voltage Lock-out threshold, MT8103 can be enabled by pulling the EN pin to above 1.5V. MT8103 is disabled if the EN pin is pulled below 0.4V. This pin has a pull-down resistor of typically 1MΩ to GND.

Soft Start

MT8103 has built-in soft start of 1ms. During the soft start period, output voltage is ramped up linearly to the regulation voltage, independent of the load current level and output capacitor value.

Current Limit and Hiccup Mode

MT8103 has cycle-by-cycle HS current limit protection to prevent inductor current from running away. Once HS current limit is triggered, MT8103 will turn on LS and wait for the inductor to drop down to a pre-determined level before the HS can be turned on again. If this current limit condition is repeated for a sustained long period of time, MT8103 will consider it over-load or short circuit. Either way, MT8103 will enter hiccup mode, where it stops switching for a pre-determined period of time before automatically re-try to start up again. It always starts up with soft-start to limit inrush current and avoid output overshoot.

Power Good Indication

MT8103 has open drain Power GOOD indicator PGOOD pin. When PGOOD is connected with external pull up resistor, it will be pulled up if output voltage is higher than 90% of regulation, otherwise PGOOD is pulled down by the internal open drain NMOS.

APPLICATION INFORMATION

Setting the Output Voltage

External feedback resistors are used to set the output voltage. For any chosen R1, the bottom feedback resistor R2 can be calculated as:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{0.6} - 1}$$

Inductor Selection

The recommended inductor value for MT8103 is 1.0uH. Usually the inductor value is chosen to satisfy a desired ripple current:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{SW} \cdot \Delta I}$$

where ΔI is the inductor ripple current.

With the chosen ΔI, the peak inductor current will be:

$$I_{PK} = I_{LOAD} + \frac{1}{2} \cdot \Delta I$$

Input Bypass Capacitor Selection

The input current to the step-down converter is discontinuous with very sharp edges, therefore an input bypass capacitor is required. For best performance, it's recommended to use low ESR ceramic capacitors and place them as close to the input pin as possible. For lowest temperature variations, use X5R or X7R dielectric ceramic capacitors.

The RMS current of the input capacitor is approximately:

$$I_{CIN\_RMS} = I_{OUT}\sqrt{D(1-D)}$$

From the equation, it can be seen that the highest RMS current occurs when D is 0.5:

$$I_{CIN\_RMS} = \frac{1}{2} I_{OUT}$$

Choose the capacitor with RMS current rating higher than 1/2 I_{OUT}

The power dissipation on the input capacitor can be estimated with the RMS current and the ESR resistor.

Electrolytic or tantalum capacitors can also be used, but due to their significantly higher ESR, a small size ceramic capacitor should be placed as close to the IC as possible.

The voltage ripple on the input capacitor, neglecting the ESR impact, can be calculated as:

$$\Delta V_{CIN} = \frac{I_{LOAD}}{f_{SW} \cdot C_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot (1 - \frac{V_{OUT}}{V_{IN}})$$

Output Capacitor Selection

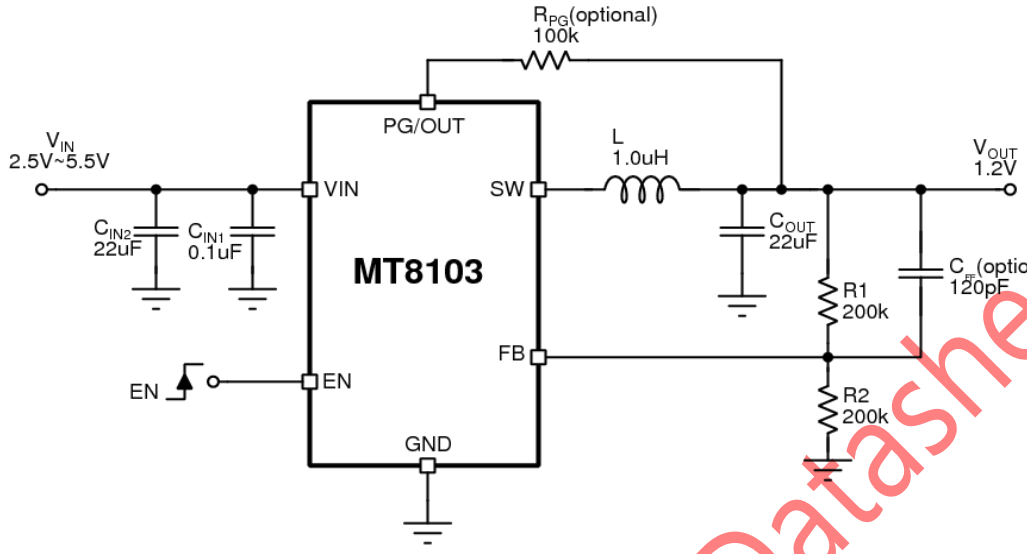
An output capacitor is required to obtain a stable output voltage. To minimize the output voltage ripple, ceramic capacitors should be used, and the ripple voltage can be estimated as:

$$\Delta V_{OUT} = \frac{1}{8} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot \frac{V_{OUT}}{L} \cdot \frac{1}{(f_{SW})^2 \cdot C_{OUT}}$$

If electrolytic or tantalum capacitors are used, the ESR will dominate the output voltage ripple:

$$\Delta V_{OUT} = (1 - \frac{V_{OUT}}{V_{IN}}) \cdot \frac{V_{OUT}}{f_{SW} \cdot L} \cdot R_{ESR}$$

Application Schematic



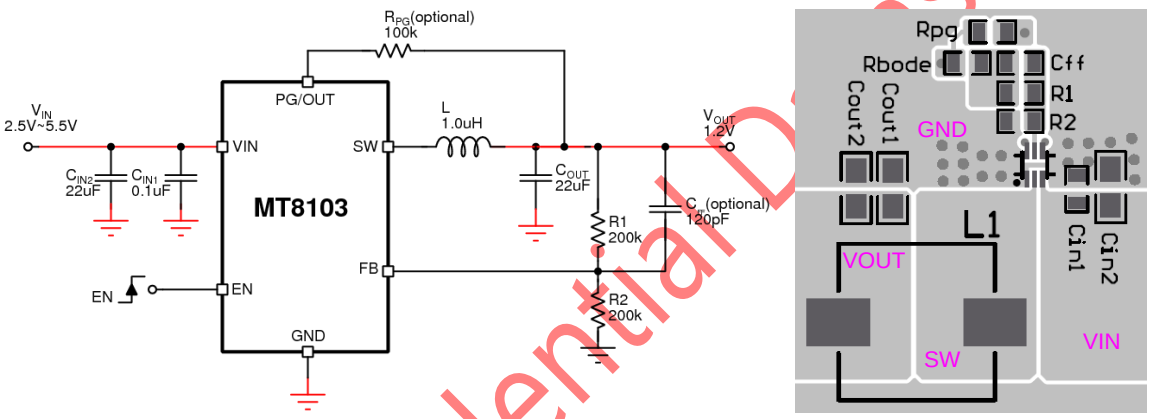
EVB BOM List

Qty	Ref	Value		Description	Package
1	C_{IN1}	0.1μF		Ceramic Capacitor, 16V, X7R	0603
1	C_{IN2}	22μF		Ceramic Capacitor, 16V, X5R	0805
1	C_{OUT}	22μF		Ceramic Capacitor, 16V, X5R	0805
1	R1	Vout=0.8V	100kΩ	Resistor, ±1%	0603
		Vout=1.0V	200kΩ		
		Vout=1.2V	200kΩ		
		Vout=1.8V	200kΩ		
		Vout=3.3V	200kΩ		
1	R2	Vout=0.8V	300kΩ	Resistor, ±1%	0603
		Vout=1.0V	300kΩ		
		Vout=1.2V	200kΩ		
		Vout=1.8V	100kΩ		
		Vout=3.3V	44.3kΩ		
1	C_{FF}	120pF		Ceramic Capacitor, 16V, X7R	0603
1	L	1.0uH		L=1uH (WE74439384010, 7.9×7.6×3.2mm, DCR=3.9mΩ)	SMD
1	R_{PG}	100kΩ		Resistor, ±1%	0603
1	U1	MT8103		DC-DC Buck Converter	SOT563

PCB Layout Recommendation

The physical design of the PCB is the final stage in the design of power converter. If designed improperly, the PCB could radiate excessive EMI and contribute instability to the power converter. Therefore, following the PCB layout guidelines below can ensure better performance of MT8103.

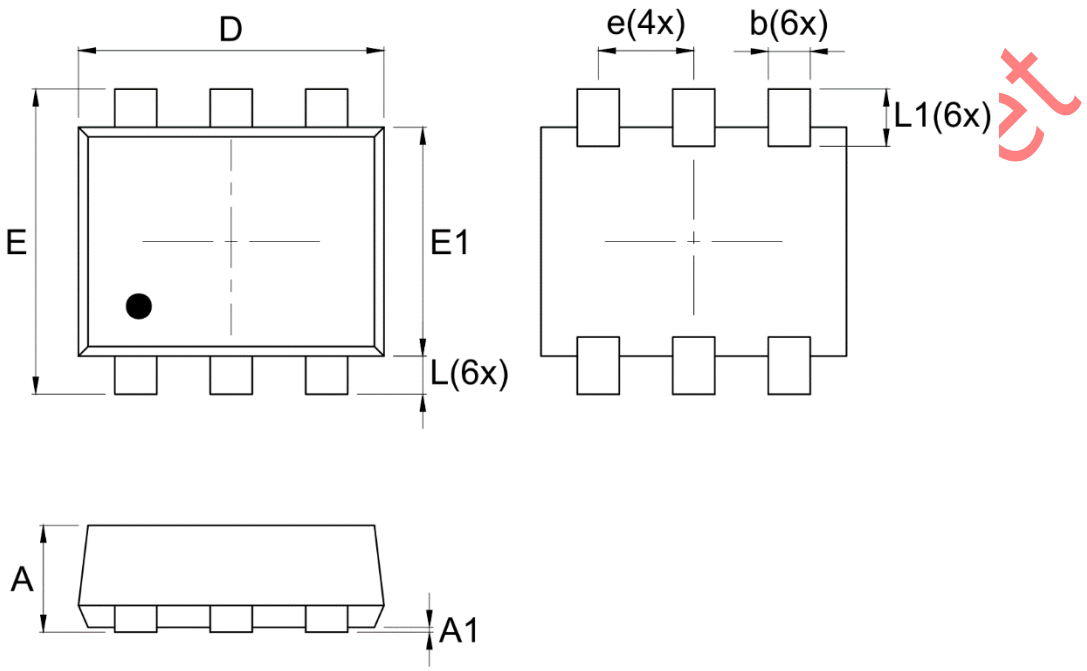
- The loop (Vin-SW-L-Cout-GND) indicates a high current path. The traces within the loop should be kept as wide and short as possible to reduce parasitic inductance and high-frequency loop area. It is also good for efficiency improvement.
- Input capacitor as close as possible to the IC Pins (Vin and GND) and the input loop area should be as small as possible to reduce parasitic inductance, input voltage spike and noise emission.
- Feedback components (R_1, R_2 and C_{FF}) should be routed as far away from the inductor and the SW Pin as possible to minimize noise and EMI issue.



PACKAGING INFORMATION

SOT563 Outline Dimensions

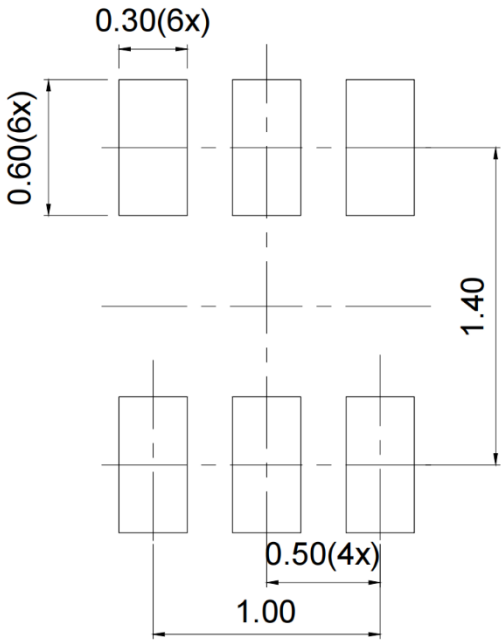
Unit: inches/mm



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.52	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
b	0.17	0.27	0.007	0.011
D	1.50	1.70	0.059	0.067
E	1.50	1.70	0.059	0.067
E1	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
L1	0.20	0.40	0.008	0.016

LAND PATTERN INFORMATION

SOT563_6L

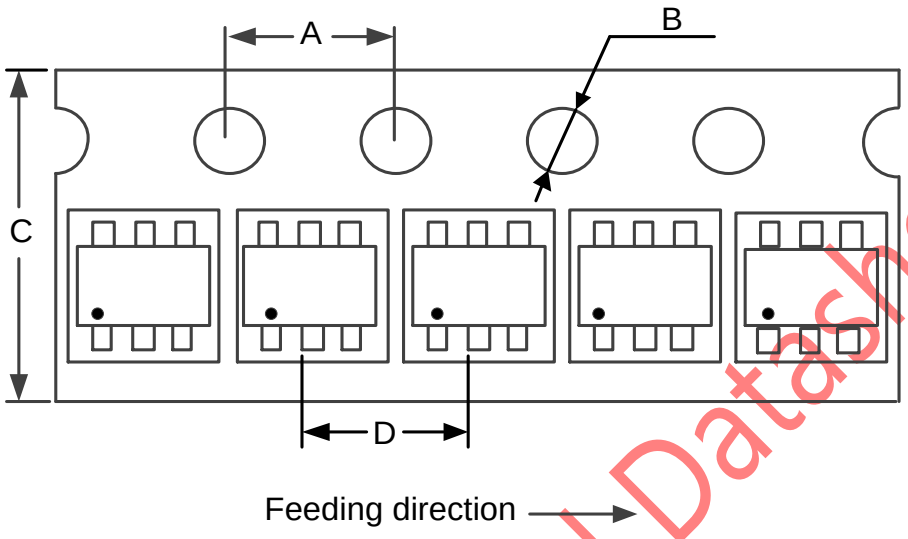


Note:

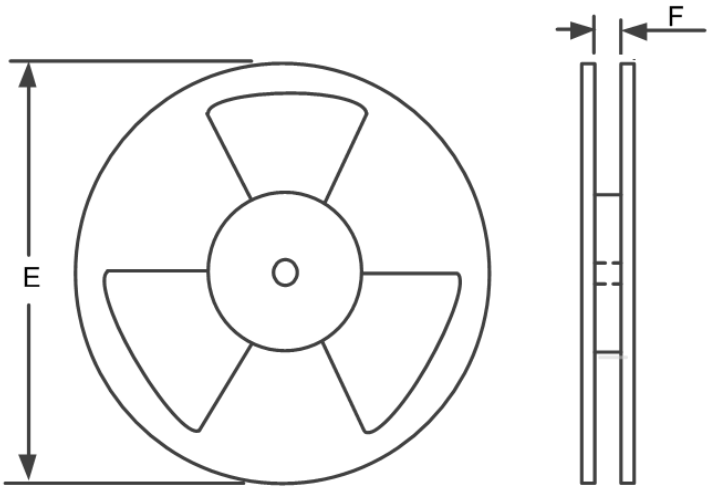
- Dimensions in mm.
- For reference only.

CARRIER TAPE & REEL DIMENSIONS

1. Orientation / Carrier Tape Information:



2. Reel Information:



3. Dimension Details:

PKG Type	A	B	C	D	E	F	Q'ty/Reel
SOT563_6L	4.0 mm	1.5mm	8.0mm	4.0mm	7.0inch	9.5mm	5000

REFLOW PROFILE

Classification Of IR Reflow Profile

Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts_{min} to Tp)	1~2℃/second, 3℃/second max.
Preheat & Soak -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time($ts_{min}$to $tsts_{max}$)	 150℃ 200℃ 60~120 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60~150 seconds
Peak Temperature(Tp)	See Classification Temp intable1
Time within 5℃of actual Peak Temperature(tp)	30 seconds max.
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

* Tolerance for peak profile Temperature(T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p)is defined as a supplier minimum and a user maximum.

Table 1. Pb-freeProcess –Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6mm	260℃	260℃	260℃
1.6mm–2.5mm	260℃	250℃	245℃
2.5mm	250℃	245℃	245℃

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.